# DEVELOPMENT OF A COMPACT, BROADBAND FET LINEARIZER FOR SATELLITE USE

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## ABSTRACT

A small sized, high performance linearizer has been developed. This linearizer consists of only one FET and simple matching circuits and is useful in a very broadband from 2 to 12 GHz. The linearizer has been adopted into an SSPA for the GLOBALSTAR program, and a 2dB NPR improvement has been achieved at the 3dB output backoff point.

## INTRODUCTION

To accommodate the increasing demand for mobile and satellite communication systems, it is becoming a key technology to transmit a number of carriers simultaneously through a common power amplifier. The power amplifier used for such communication systems should be operated in the saturated region to achieve high efficiency. However, in this saturated region, the amplifier's amplitude and phase distortion increases significantly and causes crosstalk between channels due to intermodulation. To achieve low distortion performance and high efficiency simultaneously, linearization technology which can achieve low distortion performance with small back-off from saturated power has been adopted. Especially in SSPAs for satellite use, a number of predistortion type linearizer designs have been reported[1,2,3]. However, owing to complex circuits, their sizes are large and useful bandwidth is small.

Some types of miniature linearizer have been reported, such as a gate grounded FET linearizer[4] or that applying a large source inductance[5]. But all of them have disadvantages, such as narrow bandwidth and difficulty of tuning.

In this paper, a new type of linearizer is discussed which has been developed based on the fact that a source grounded FET's amplitude and phase characteristics are mainly dependent on the drain to source resistance(Rds) variation. This linearizer consists of only one FET and bias circuits. Because of its simple circuit, the linearizer can be operated over a 10GHz bandwidth and has good thermal stability. Furthermore, the characteristics of this linearizer can be easily tuned using its gate bias condition.

This linearizer has been adopted into a 50W output type SSPA at 7GHz, which is designed for the GLOBALSTAR program, and a 2dB NPR improvement has been achieved at the 3dB output backoff point.

## DEVELOPMENT OF LINEARIZER

A source grounded and no drain biased FET's equivalent circuit is shown in Fig.1[6]. This circuit shows how the drain to source resistance(Rds) varies with the gate to source capacitance (Cgs). In the case that the FET's operating point changes from the linear region to saturation, the value of Rds increases[7]. As a result, the FET would show increasing gain and negative phase characteristics as shown in Fig.2. This performance is just the opposite of a high power FET's, and can be used as a linearizer.

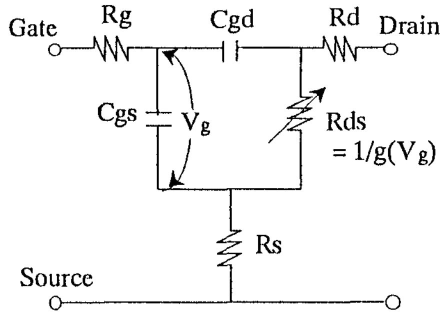


Figure 1: Source grounded and no gate biased FET equivalent circuit

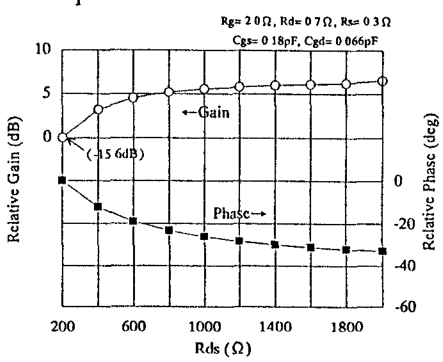


Figure 2: FET's amplitude and phase characteristics with Rds variation (calculation)

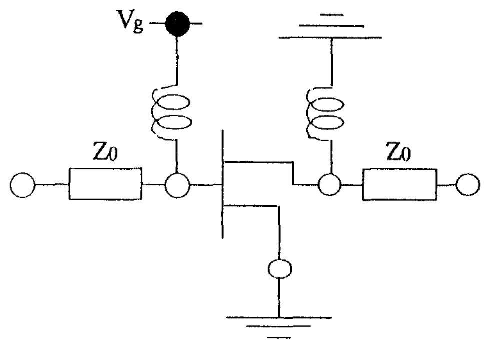


Figure 3: Schematic diagram of the linearizer

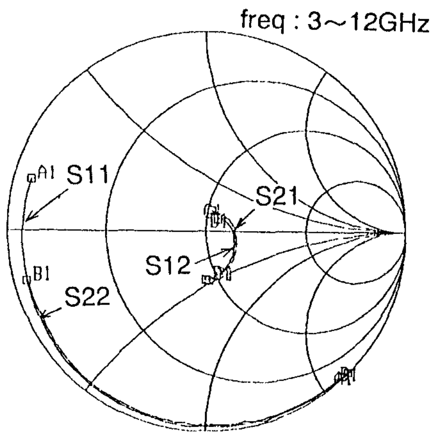


Figure 4: Small signal S-parameter of FET

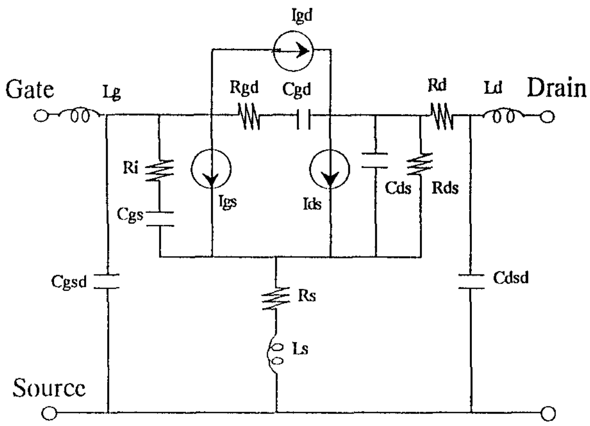


Figure 5: Large signal equivalent circuit of FET

Fig.3 shows a schematic diagram of a developed linearizer's construction. This linearizer consists of only one GaAs MESFET (MITSUBISHI MGF1423 ; Wg=240$\mu$m, Psat=20mW) and both input and output matching circuits.

As the first step of the design, the FET's small signal S-parameters without drain bias (Vds=0V) were measured as shown in Fig.4. Judging from the result that $S_{11}$ equals $S_{22}$ and $S_{12}$ equals $S_{21}$, this FET can be considered to have symmetrical characteristics.

Using the above S-parameters and DC characteristics, the large signal equivalent circuit has been fitted as shown in Fig.5. Under -0.4V gate bias condition, a 2dB increased gain and a negative 40degree phase performance can be seen as shown in Fig.6.

Fig.7 shows a photograph of a developed linearizer for 7GHz use. Total size including matching circuits is 14x14mm.

Fig.8 shows the measured amplitude and phase characteristics with varying FET gate bias. At Vgs=-0.4V, the linearizer has 3dB increased gain and about 30degree negative phase performance, this shows good agreement with the above calculation result. Additionally, the linearizer's performance can be tuned easily by varying the gate bias.

Fig.9 shows the linearizer's measured amplitude and phase characteristics with varying input signal frequency. From 2 to 12GHz, over a 10GHz bandwidth, this linearizer shows the same performance. Judging from this result, this linearizer has an extremely broadband operational range.

Fig.10 shows the linearizer's performance at each temperature, from -10 to +75°C. The variation of its amplitude and phase are less than 1dB and 5degree respectively, so it can be considered that this linearizer has good thermal stability.

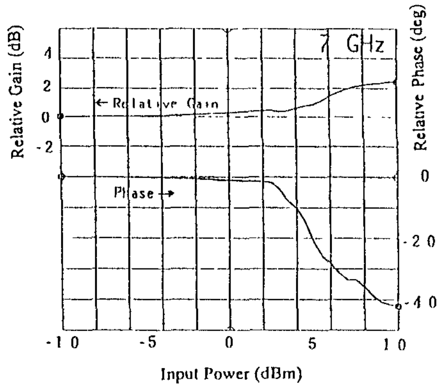


Figure 6: Amplitude and phase characteristics of the linearizer (calculation)

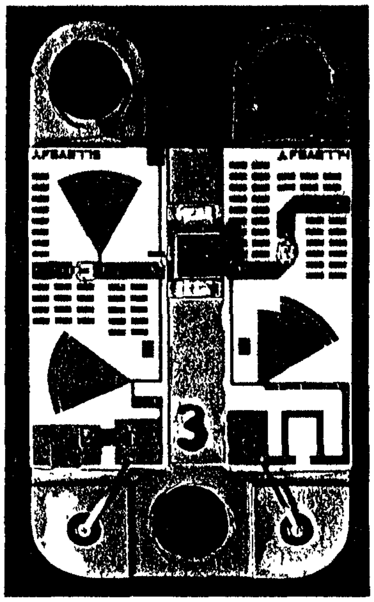

Figure 7: Photograph of the linearizer

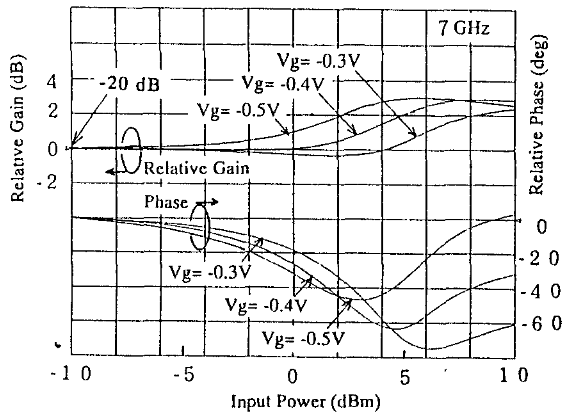


Figure 8: Linearizer's performance with Vg variation (measured)

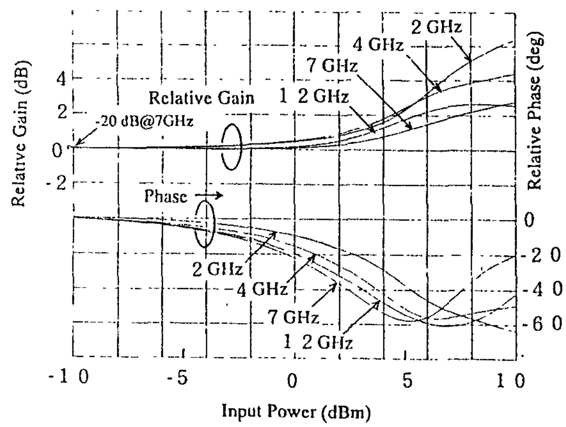


Figure 9: Linearizer's frequency performance (measured)

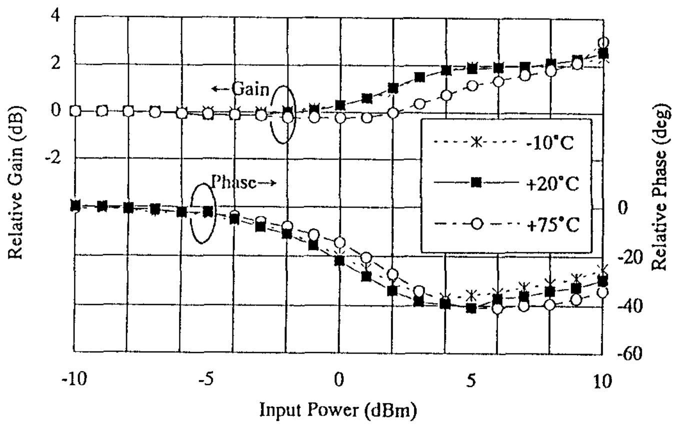


Figure 10: Linearizer's thermal performance (measured)

## LINEARIZED HIGH POWER AMPLIFIER

This linearizer has been applied to an SSPA of 50W saturated output power at 7GHz, which was designed for the GLOBALSTAR program. A block diagram of the linearized power amplifier is shown in Fig.11. It consists of the high power amplifier, the linearizer, the isolator and an attenuator. The attenuator is controlled by a ROM to achieve good temperature compensation. A High power GaAs FET (MGFC44V) is used in the last stage to achieve high power efficiency. This FET is internally matched and consists of matching circuits and 4 FET chips of which gate width is 18.9mm. The FET obtains power-added efficiency of 45±3% and saturated output power of 44.3±0.4 dBm.

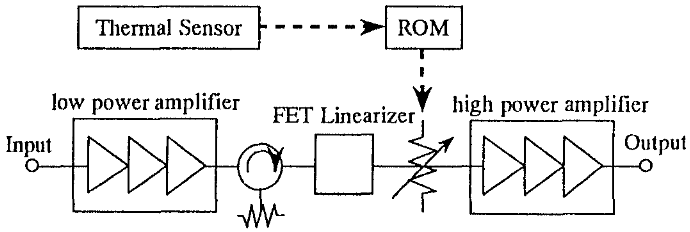


Figure 11: Block diagram of the linearized amplifier

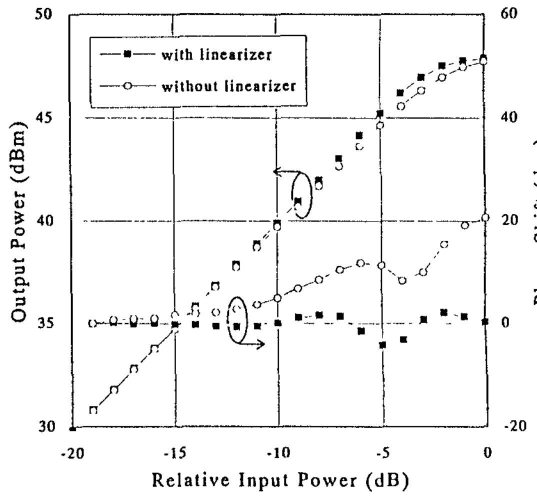


Figure 12: Amplitude and phase performance of SSPA with and without linearizer (measured)

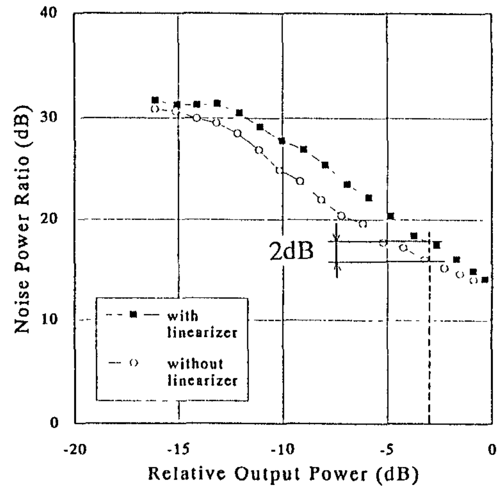


Figure 13: NPR performance of SSPA with and without linearizer (measured)

To evaluate the effect of the linearizer, both linearized and non-linearized SSPAs' performance have been measured. Fig.12 shows the measured result; the solid black square is the linearized performance and the circle is the non-linearized performance. By including the linearizer, compensation of about 1dB gain and 15degree phase has been achieved.

Fig.13 shows the NPR performance of both cases. The NPR has been improved over a 15dB dynamic range, and 2dB improvement is seen at the 3dB output backoff point. To achieve the same NPR without using a linearizer, an additional 2dB of output power would be necessary and this effect corresponds to about 60W power consumption degradation.

This linearized SSPA has also completed environmental and electro-magnetic compatibility tests for satellite use, and is expected to be used in the GLOBALSTAR program satellites.

## CONCLUSION

A compact and broadband FET linearizer has been developed for satellite use. It is composed of a source grounded FET and matching circuits, which has broadband performance and good thermal stability, and can be easily tuned by DC bias variation. Applying this linearizer to a 7GHz SSPA, a 2dB NPR improvement at the 3dB backoff point has been achieved.

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